Docket: TSMC 98 - 684/685/688C
S/N: 09/418,031

1765

To: Commissioner of Patents and Trademarks
Washington, D.C. 20231

From: George O. Saile, Reg. No. 19,572
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Subject:

Serial No.: 09/418,031	Filed: 10/14/99
Inventor: Syun-Ming Jang	
Title: Modified Pad for Copper/Low-K	
Group Art Unit: 1765	Examiner: Vinh, Lan
Attorney Docket: TSMC 98-684/685/688	

RESPONSE TO PATENT OFFICE ACTION

Dear Sir:

In response to the office action dated 05/09/03, please consider the following remarks:

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on August 11, 2003.

Signature/Date 8/11/03

Stephen B. Ackerman

Reg. No. 37,761

In the Claims

Amendments to the claims:

1. (currently amended) A method for forming a patterned microelectronics layer comprising:

providing a substrate having at least one conductor stud within a contact region formed therein;

forming on the at least one conductor stud a first lower sub-layer and a second upper sub-layer to provide a composite etch stop layer;

forming over the composite etch stop layer an inter-level metal dielectric (IMD) layer;

forming over the IMD layer a photoresist mask layer pattern of an interconnection line trench pattern centered over the contact layer and transferring the pattern by etching while employing a first etching method through the IMD layer and the second upper sub-layer of the composite etch stop layer to the first lower sub-layer of the composite etch stop layer; and

etching while employing a second etch method the first lower sub-layer from the trench pattern for the interconnection lines.

2. (original) The method of Claim 1 wherein by employing the first lower sub-layer there is avoided etching of the contact region within the first etching method.

3. (currently amended) The method of Claim 1 wherein the first lower sub-layer has a higher etch rate in the second etching method than the contact region;.

4. (original) The method of Claim 1 wherein forming a damascene multi-layer conductor interconnection layer is accomplished by the method further comprising:

forming a barrier metal layer over the patterned substrate; and

filling the trench pattern with a conductor material to complete the damascene multi-layer conductor interconnection layer structure.

5. (original) The method of Claim 1 wherein the microelectronics layer is selected from the group consisting of:

microelectronics conductor layers;

microelectronics semiconductor layers;

microelectronics dielectric layers.

6. (original) The method of Claim 1 wherein the substrate is a substrate employed within a microelectronics fabrication selected from the group consisting of:

integrated circuit microelectronics fabrications;

charge coupled device microelectronics fabrications;

solar cell microelectronics fabrications;

light-emitting diode microelectronics fabrications;

ceramic substrate microelectronics fabrications; and

flat panel display microelectronics fabrications.

7. (original) The method of Claim 1 wherein the first lower sub-layer is formed employing a silicon oxide dielectric material formed employing plasma enhanced chemical vapor deposition (PECVD).

8. (original) The method of Claim 1 wherein the upper second sub-layer is formed employing a silicon oxynitride dielectric material deposited employing plasma enhanced chemical vapor deposition (PECVD).

9. (original) The method of Claim 1 wherein the contact region via conductor stud layer material is formed employing tungsten metal.

10. (original) The method of Claim 1 wherein the inter-level metal dielectric (IMD) layer is formed employing silicon oxide dielectric material employing chemical vapor deposition (CVD).

11. (previously amended) The method of Claim 4 wherein the said conductor material is copper metal.

12. (currently amended) A method for forming a patterned microelectronics layer comprising:

providing a substrate having a contact region of tungsten metal conductor studs formed therein;

forming ~~over~~ on the substrate a first lower organic polymer sub-layer and a second upper sub-layer to provide a composite etch stop layer;

forming over the composite etch stop layer a blanket inter-level metal dielectric (IMD) layer;

forming over the blanket IMD layer a photoresist mask layer pattern of an interconnection line trench pattern centered over the contact region and transferring the pattern while employing a first etch method through the blanket IMD layer and the second upper sub-layer of the composite etch stop layer to the first lower organic polymer sub-layer of the composite etch stop layer; and

stripping the photoresist mask pattern layer and simultaneously etching the first lower organic polymer sub-layer to complete the formation of the interconnection trench pattern centered over the tungsten metal stud contact region.

13. (original) The method of Claim 12 wherein by employing the first lower organic polymer sub-layer there is avoided the etching of the tungsten metal stud contact region within the first etch method.

14. (original) The method of Claim 12 wherein forming a damascene multi-layer conductor interconnection layer structure is accomplished by the method further comprising:

forming a barrier metal layer over the substrate; and

filling the interconnection trench pattern with a conductor material to complete the damascene multi-level conductor interconnection layer structure.

15. (original) The method of Claim 12 wherein the semiconductor substrate is a silicon semiconductor substrate.

16. (original) The method of Claim 12 wherein the first lower organic polymer sub-layer is formed employing a low dielectric constant spin-on-polymer (SOP) dielectric material.

17. (original) The method of Claim 12 wherein the second upper sub-layer is formed employing chemical vapor deposition (CVD) of silicon containing dielectric material.

18. (original) The method of Claim 12 wherein the inter-level metal dielectric (IMD) layer is formed of silicon oxide dielectric material employing chemical vapor deposition (CVD).

19. (previously amended) The method of Claim 14 wherein the conductor material employed to fill the interconnection trench is copper metal.

20. (previously amended) The method of Claim 14 wherein the barrier metal layer is formed employing tantalum nitride (TaN).

21. (previously added) The method of claim 1, wherein:

(1) the first etching method employs a mixture of:

CF4;

CHF3; and

oxygen

as etching gasses; and

(2) the second etch method employs argon as a sputtering gas.

22. (previously added) The method of claim 12, wherein:

(1) the first etching method employs a mixture of:

CF4;

CHF3; and

oxygen

as etching gasses; and

(2) wherein etching of the first lower organic polymer sub-layer employs argon as a sputtering gas.

Remarks

Examiner Vinh is thanked for the thorough Office Action.

In the Claims

Claim 1 has been currently amended to correct an informality, i.e. by adding "and" before the last sub-paragraph. This amendment does not narrow the claim and is believed not to be related to patentability.

Claim 3 has been currently amended to corect an informality, i.e. by replacing the semicolon at the end of the claim with a period. This amendment does not narrow the claim and is believed not to be related to patentability.

Claim 12 has been currently amended to indicate that "a first lower organic polymer sub-layer and a second upper sub-layer" are formed "on the substrate ... to provide a composite etch stop layer."

Claim Rejections

The Rejection Of Claims 12 To 20 Under 35 U.S.C. §103(a) as Being Unpatentable Over Zhao (U.S. Patent No. 6,100,184) In View Of Huang et al. (U.S. Patent No. 6,191,484) And Further In View Of Cronin et al. (U.S. Patent No. 5,759,911)

The rejection of claims 12 to 20 under 35 U.S.C. §103(a) as being unpatentable over Zhao (U.S. Patent No. 6,100,184) (the '184 Zhao Patent) in view of Huang et al. (U.S. Patent No. 6,191,484) (the '484 Huang Patent) and further in view of Cronin et al. (U.S. Patent No. 5,759,911) (the '911 Cronin) is acknowledged.

The Rejection Of Claim 22 Under 35 U.S.C. §103(a) as Being Unpatentable Over Zhao (U.S. Patent No. 6,100,184) In View Of Huang et al. (U.S. Patent No. 6,191,484) And Cronin et al. (U.S. Patent No. 5,759,911) And Further In View Of Qiao (U.S. Patent No. 6,372,634)

The rejection of claim 22 under 35 U.S.C. §103(a) as being unpatentable over Zhao (U.S. Patent No. 6,100,184) (the '184 Zhao Patent) in view of Huang et al. (U.S. Patent No. 6,191,484) (the '484 Huang Patent) and Cronin et al. (U.S. Patent No. 5,759,911) (the '911 Cronin) and further in view of Qiao (U.S. Patent No. 6,372,634) (the '634 Qiao Patent) is acknowledged.

Claim 12 has been currently amended to indicate that "a first lower organic polymer sub-layer and a second upper sub-layer" are formed "on the substrate ... to provide a composite etch stop layer." Claim 12 is therefore allowable as the Examiner's reasoning for allowance of claims 11 to 20 and 21 is because the cited prior art of record fails to disclose forming on the at least on conductor stud a first lower sub-layer and a second upper sub-layer to provide a composite etch stop layer whereas the closes prior art of Huang discloses forming a first sub-layer 24 and a second sub-layer 26 to provide a composite etch stop layer over the conductor stud 12.

Claims 13 to 20 and 22 depend from currently amended independent claim 12 and are believed to distinguish over the combination for the reasons previously cited.

Allowable subject matter

The allowance of claims 1 to 11 and 21 is gratefully acknowledged.

Applicants acknowledge that the Examiner's reasoning for allowance of claims 11 to 20 and 21 is because the cited prior art of record fails to disclose forming on the at least on conductor stud a first lower sub-layer and a second upper sub-layer to provide a composite etch stop layer whereas the closes prior art of Huang discloses

forming a first sub-layer 24 and a second sub-layer 26 to provide a composite etch stop layer over the conductor stud 12.

Therefore claims 1 to 22 are submitted to be allowable over the cited references and reconsideration and allowance are respectfully solicited.

CONCLUSION

In conclusion, reconsideration and withdrawal of the rejections are respectively requested. Allowance of all claims is requested. Issuance of the application is requested.

It is requested that the Examiner telephone Stephen G. Stanton, Esq. (#35,690) at (610) 296 - 5194 or the undersigned attorney/ Stephen B. Ackerman, Esq. (#37,761) at (845) 452 - 5863 if the Examiner has any questions or issues that may be resolved to expedite prosecution and place this Application in condition for Allowance.

Respectively submitted,

Stephen B. Ackerman

Reg. No. 37,761